IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Mei	Examiner:	Tran, Thanh Y
Serial No.:	10/769,127	Group Art Unit:	2892
Filed:	1/30/2004	Docket No.:	200209576-1
Title:	FORMING A SEMICONDUCTOR DEVICE		

REPLY BRIEF UNDER 37 C.F.R. §41.37

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This Reply Brief is submitted in response to the Examiner's Answer filed on October 10, 2008, rejecting claims 1-10, 13-20, 22 and 23 of the above-identified application as set forth in the Final Office Action mailed March 13, 2008.

Appellant respectfully requests consideration and reversal of the Examiner's rejection of pending claims 1-10, 13-20, 22 and 23.

STATUS OF CLAIMS

In a Final Office Action mailed March 13, 2008, claims 1, 3, 13, 14 and 17 were finally rejected. Claims 1-10, 13-20, 22 and 23 are pending in the application, and are the subject of the present Appeal.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

i. Claims 1 and 13 stand rejected under 35 U.S.C. §102(b) as being anticipated by Dai (US Patent 5,877,076).

ii. Claims 3, 14 and 17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Dai in view of Taussig. et al., (US 6,861,365).

ARGUMENT

I. The Applicable Law

U.S.C. § 102

We respectfully remind the Examiner that in order to anticipate a claim, US Patent 5,877,076 to Dai (hereinafter *Dai*) must teach **every element of the claim** and ***"the identical invention must be shown in as complete detail as contained in the ... claim."*** *MPEP 2131* citing *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987) and *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989) (emphasis added).

U.S.C. § 103

The standard for making an obviousness rejection is currently set forth in MPEP 706.02(j):

> To establish a *prima facie* case of obviousness, *three basic criteria must be met*. **First**, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. **Second**, there must be a reasonable expectation of success. **Finally**, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The ***teaching or suggestion*** to make the claimed combination **and** the ***reasonable expectation of success* must *both be found in the prior art*, and not *based on applicant's disclosure.*** (emphasis and formatting added) MPEP § 2143, *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)
>
> The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a ***convincing line of reasoning*** as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). (emphasis added).

See also, KSR International Co. v. Teleflex Inc., No. 04-1350, 550 U.S. ___ (2007).

As noted above, the PTO has the burden of establishing a prima facie case of obviousness under 35 USC §103. The Patent Office must show that some reason to combine the elements with some rational underpinning that would lead an individual of ordinary skill in the art to combine the relevant teachings of the references. *KSR International Co. v. Teleflex Inc.*, No. 04-1350, 550 U.S. ___ (2007); *In re Fine*, 837 F.2d 1071, 1074 (Fed. Cir. 1988). Therefore, a combination of relevant teachings alone is insufficient grounds to establish obviousness, absent some reason for one of ordinary skill in the art to do so. *Fine* at 1075.

a. Rejection of Claims 1 and 13 under 35 U.S.C. §102(b) (076 References)

The Applicant respectfully traverses the rejection of **Claims 1** and **13** because all of the elements of independent **Claims 1** and **13** are not disclosed by *Dai*, as emphasized by the recited claim elements set forth below.

> Independent **Claim 1** recites a method for forming a semiconductor device comprising:
> forming a 3-dimensional (3D) pattern in a substrate; and
> depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device.
>
> Independent **Claim 13** recites a system for forming a semiconductor device comprising:
> means for forming a 3-dimensional (3D) pattern in a substrate; and
> means for depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device.

The Examiner states that the *Dai* reference anticipates the present invention. Applicant respectfully disagrees and asserts that ***the Dai reference does not disclose forming a 3-dimensional (3D) pattern in a substrate as recited in claims 1 and 13 of the present invention.*** (Emphasis added.) *Dai* discloses a method for forming dual

damascene interconnections in semiconductor chips through the use of opposite type two-layered photoresist process. A silicon substrate is provided having a composite layer comprising a first layer of dielectric separated from a second layer of dielectric by an intervening intermediate layer of silicon nitride. Then, a layer of positive (P-type) chemical amplification resist (CAR) is deposited over the composite dielectric layer. The P-type resist is next line patterned by exposing and developing it through a dark field mask. This is followed by cross-linking the remaining P-type resist by performing a hard-bake. An opposite polarity, namely, a negative (N-type) CAR is next formed over the opposite P-type resist, and hole patterned through a clear field mask.

Because of cross-linking, the P-type resist is not affected during hole patterning of the opposite N-type resist. The hole pattern is next transferred by dry etching into the top dielectric layer and then into the intervening silicon nitride layer in the composite layer. The line pattern in the P-type CAR layer is etched into the top dielectric layer at the same time the hole pattern is transferred from the top dielectric layer into the bottom dielectric layer by the same etching process. The photoresist layers are then removed and the dual damascene structure thusly formed is filled with metal forming the line trench and hole interconnection on the semiconductor substrate.

While *Dai* discloses a substrate layer (110), the ***Dai reference does not disclose forming a 3-dimensional (3D) pattern in a substrate as recited in claims 1 and 13 of the present invention***. The Examiner asserts that *Dai* discloses forming a 3-dimensional pattern (161', 151') in a substrate. Applicant respectfully disagrees. ***The pattern(s) 161', 151' that the Examiner references are not formed in the substrate (110).*** The patterns are formed in the composite dielectric insulation layers 120, 130, 140 (see Figure 3j, Dai). Consequently, *Dai* does not teach or suggest forming a 3-dimensional (3D) pattern in a substrate as recited in claims 1 and 13 of the present invention.

Since *Dai* does not teach or suggest forming a 3-dimensional (3D) pattern in a substrate as recited in claims 1 and 13 of the present invention, the *Dai* reference does

not teach or suggest each element of independent **Claims 1** and **13**. Accordingly, the rejection of **Claims 1** and **13** under **35 U.S.C. §102(b)** should be withdrawn.

b. Rejections of Claims 3, 14 and 17 under 35 U.S.C. §103(a) (076, 365 References)

The Applicant respectfully traverses the rejection of **Claims 3, 14** and **17** as being unpatentable over US Patent **5,877,076** to *Dai* in view of US Patent ***6,861,365*** to *Taussig et al.* **Claims 3, 14** and **17** depend from independent **Claims 1** and **13** respectively and inherit all of their limitations. Therefore, **Claims 3, 14** and **17** are also patentably distinct in light of US Patent **5,877,076** to *Dai* in view of US Patent ***6,861,365*** to *Taussig et al.* and the rejections of **Claims 3, 14** and **17** under **35 U.S.C. §103(a)** ought to now be withdrawn.

Allowable Subject Matter

The Examiner has indicated that **Claims 2, 4-10, 15-16, 18-20** and **22-23** are objected to as being dependent upon a rejected base claim, but would be allowed if rewritten in independent form including all of the limitations of the base claim. Applicant appreciates Examiner's findings. In light of the above remarks concerning the lack of anticipation and failure to properly support a finding of obviousness, applicant contends that the allowability of **Claims 2, 4-10, 15-16, 18-20** and **22-23** remains unchanged, but that a re-write for independent standing is no longer necessary.

Response to Examiner's Answer

The Examiner asserts that the Appellant's argument has been fully considered but it is not persuasive because the Dai reference clearly discloses in figures 3i-3k a method and a corresponding apparatus comprising a 3-D pattern (as indicated at 161' and 151') is formed in a substrate (a substrate comprises layers (160, 150, 140, 130,

120, 110)). Thus, the 3D pattern(s) created by 161' and 151' in figures 3i-3k of *Dai* is in the substrate (160, 150, 140, 130, 120, 110). Figures 3i-3k of *Dai* are reproduced herein below:

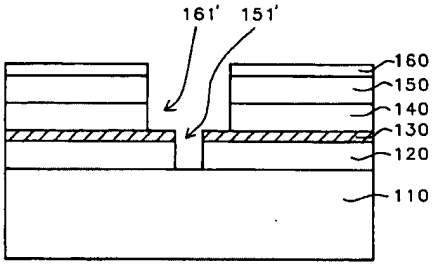


FIG. 3i

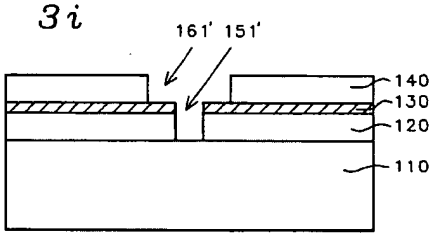


FIG. 3j

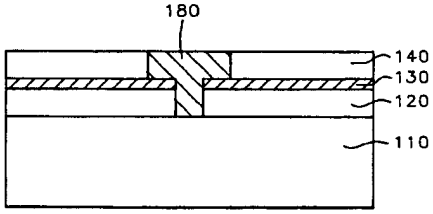


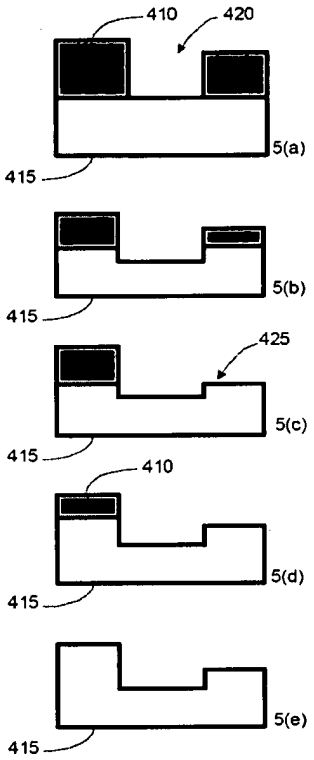
FIG. 3k

Appellant asserts that according to *Dai*, layer 110 above is a substrate, see *Dai* col. 5 lines 47-51 reproduced herein below:

> ...***substrate (110)***, preferably silicon, is provided with a composite tri-layer dielectric insulation comprising bottom and top layers (120) and (140), respectively, and a middle layer (130). A layer of photoresist (150) is next formed on the composite layer... (Emphasis added.)

Appellant asserts that the substrate 110 is clearly distinct from the insulation layers 120-140 and the photoresist layers 150, 160. As such, Appellant asserts that the pattern 151', 161' are respectively formed in the insulation and photoresist layers 120-160, ***not the substrate layer 110.***

Appellant stipulates that the present invention recites forming a 3-dimensional (3D) pattern ***in a substrate.*** This is clearly shown in Figures 5(a-e) of the present invention reproduced herein below:



Here, element 415 is the substrate. As can clearly be seen above (e.g. Figure 5(e)), a pattern is formed ***in the substrate 415.***

The Examiner purports that a substrate can be a multi-layer substrate or comprise more than one layer as shown in figure 1(A) of the Chikagawa reference (US 2007/0184251). This may be true, however the *Dai* reference discloses a single substrate layer 110 in conjunction with insulation and photoresist layers 120-160, not a multilayer substrate. ***Nonetheless, neither the Dai reference nor the Chikagawa reference discloses forming a 3D pattern in a substrate as recited in independent Claims 1 and 13.***

CONCLUSION

For the above reasons, Appellants respectfully submit that the cited references neither anticipate nor render obvious claims of the pending Application. The pending claims distinguish over the cited references, and therefore, Appellants respectfully submit that the rejections must be withdrawn, and respectfully request the Examiner be reversed and claims 1-10, 13-20, 22 and 23 be allowed.

Any inquiry regarding this Response should be directed to Wendell J. Jones at Telephone No. (408) 938-0980. In addition, all correspondence should continue to be directed to the following address:

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Respectfully submitted,

Mei

By their attorney,

Wendell J. Jones

Date: December 5, 2008

/Wendell J. Jones/
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